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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,853	10/28/2003	Krishna K. Pappu	03-0128 81615	6739

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EXAMINER

PARIHAR, SUCHIN

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/695,853

Applicant(s)

PAPPU ET AL.

Examiner

Suchin Parihar

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– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to application 10/695,853, amendment filed on 6/2/2006. Claims 4 and 13 are amended. Claims 1-18 are pending in this application.

1. Applicant's arguments filed 6/2/2006, with respect to the rejection(s) of claim(s) 1-18 under 35 USC 103(a) have been fully considered and are persuasive. Upon further consideration, a new ground(s) of rejection is made.

Claim Objections

2. Claim 1 is objected to because of the following informalities: Starting on line 5 of claim 1, "a common signal domain" should read - -the common signal domain- -, to indicate that a corresponding list of cells is being initialized for every common signal domain in an integrated circuit design. Starting at line 7 of claim 1, "a common signal domain" should read - -one of the common signal domains- -. Starting on line 8 of claim 1, "a common signal domain" should read - -the common signal domain- -. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 10-18 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 10, it is unclear whether the computer program of claim 10 line 5 is the same as that of claim 10 line 3.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 10-18 are rejected under 35 U.S.C. 101** because: the claimed invention is directed to non-statutory subject matter. With respect to the 35 USC 101 it appears from the claim recitation of claim 10 that applicant is claiming a computer program with steps and computer programs are not statutory. The medium for embodying a computer program is not necessarily statutory as it depends on what type of medium is being referenced. In the instant case, Applicants' specification is completely silent on what type of medium is being claimed. The phrase: "for causing the computer to perform", on line 5 of claim 10, fails to provide a tangible result and therefore lacks utility.

For examination purposes and to circumvent the 35 USC 101 issues, Examiner suggests the following change to the preamble of claim 10:

- -A computer program product for grouping scan flops for scan testing comprising: a computer readable medium embodying a computer program for input to a computer; the computer program, which when executed by a computer, causing the computer to perform the steps of- -.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. **Claims 1-18 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Beausang (5,828,579) in view of Nadeau-Dostie et al. (6,457,161).

9. With respect to claims 1 and 10, Beausang teaches a method of grouping cells of an integrated circuit, which includes teaching a computer program/computer program product (description of CAD & computer system, Col 6, lines 1-42), comprising the steps of receiving as input a representation of an integrated circuit design (database [netlist] 210 that defines an IC design, acting as input to the system 205 of Figure 1B, Col 6, lines 53-55); initializing (i.e. constructing) a corresponding list of cells for a common signal domain in the integrated circuit design (constructing scan chains [i.e. lists] being of a common clock domain, Col 4, lines 5-15); selecting (i.e. accessing) a cell belonging to a common signal domain that is not included in a corresponding list of cells for a common signal domain (accessing segments [i.e. cell] that have not been assigned to a scan chain [list], Col 26, lines 60-65 & Col 27, lines 1-5); and inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15). Beausang does not specifically teach tracing steps that involve tracing a net to/from an input port of each cell connected to a signal driver. Nadeau-Dostie et al. teaches a method/computer-tool for representing a circuit that involves tracing to/from an input port of each cell connected to a signal driver to identify the cells being connected (Col 7 line 67 to Col 8

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line 57, i.e. signal tracing module). It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang.

10. With respect to claims 2 and 11, Beausang in view of Nadeau-Dostie et al. teaches all the elements of claims 1 and 10, from which the respective claims depend, as described above. Beausang also teaches repeating steps (c), (d), (e), (f) and (g) until every cell belonging to a common signal domain has been inserted in a corresponding list of cells for the common signal domain, (accessing all segments [i.e. cells] that have not already been assigned to a scan chain and partitions the segments by clock domain).

11. With respect to claims 3 and 12, Beausang in view of Nadeau-Dostie et al. teaches all the elements of claims 2 and 11 respectively, from which the respective claims depend, as described above. Beausang also teaches generating as output a corresponding list of cells for a common signal domain in the integrated circuit design (generating as output a compiler generated script file which is a complete specification of the scan configuration, Col 10, lines 50-55, also see the figure in Col 10 indicating "scan chain 1" and "scan chain 2" and the cells they each contain).

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12. With respect to claims 4 and 13, Beausang in view of Nadeau-Dostie teaches all the elements of claims 1 and 10 respectively. Beausang teaches: wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (during scan chain [i.e. list] construction, scan element name is included for each element, Col 16, lines 15-20, also see Col 10, lines 10-15).

13. With respect to claims 5 and 14, Beausang in view of Nadeau-Dostie teaches all the elements of claims 1 and 10, from which the respective claims depend, as discussed above. Beausang also teaches performing steps (b), (c), (d), (e), (f) and (g) for cells that are flip-flops in a scan chain (flip-flop is an example of a user defined segment, Col 14, lines 10-15).

14. With respect to claims 6 and 15, Beausang in view of Nadeau-Dostie teaches all the elements of claims 5 and 14, from which the claims depend respectively. Beausang teaches: performing steps (b), (c), (d), (f) and (g) for a common signal domain that is a scan clock domain (scan chains being of a common clock domain, Col 4, lines 1-15).

15. With respect to claims 7 and 16, Beausang in view of Nadeau-Dostie teaches all the elements of claims 6 and 15, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for a net that is a clock net. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for a net that is a clock net (tracing backward from the clock input port of the latch to a clock source, wherein the connection between the clock input port and the clock source is considered a "clock net", Col 8, lines 1-15).

16. With respect to claims 8 and 17, Beausang in view of Nadeau-Dostie teaches all the elements of claims 7 and 16, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for an input port that is a clock port. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for an input port that is a clock port (clock input port of a latch, Col 8, lines 10-15).

17. With respect to claims 9 and 18, Beausang in view of Nadeau-Dostie teaches all the elements of claims 8 and 17, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for a signal driver that is a clock driver. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for a signal driver that is a clock driver (clock buffer 38 driven by a clock phase PH2 [i.e. driver], Col 4, lines 35-40).

Conclusion

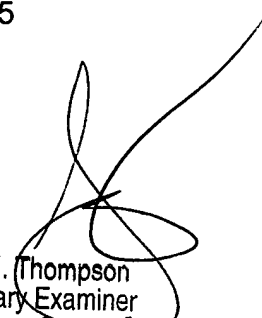
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information

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